UNIVERSITI SAINS MALAYSIA

First Semester Examination
2015/2016 Academic Session

December 2015 & January 2016

EEE 553 – Semiconductor Devices and Solid State Technology

Duration : 3 hours

Please check that this examination paper consists of **SEVEN (7)** pages printed material and **TWO (2)** pages of Appendix before you begin the examination.

Instructions: This question paper consists **SIX (6)** questions. Answer **FIVE (5)** questions. All questions carry the same marks.

1. (a) (i) What is threshold voltage?

(10 marks)

(ii) How to determine threshold voltage using Id vs Vg?

(10 marks)

(iii) What is the alternative method for threshold voltage determination?

(10 marks)

(b) Drain current of MOS transistor can be derived from $I_{ds} = WQ_{inv}v$ which is based on simple charge sheet model.

(i) Derive the basic drain current equation, $I_{dsat} = \frac{WC_{oxe}\mu_{es}}{2L}\left(V_g - V_t\right)^2$

(50 marks)

(ii) Given W/L = 10, V_{ds} = 0.15 V, Vgs= 0.7 V, V_t =0.5V, m=1, and $C_{oxe}\mu_{es}$ = 120μA/V^2

What is the region of the transistor operation ? Calculate the drain current.

(20 marks)

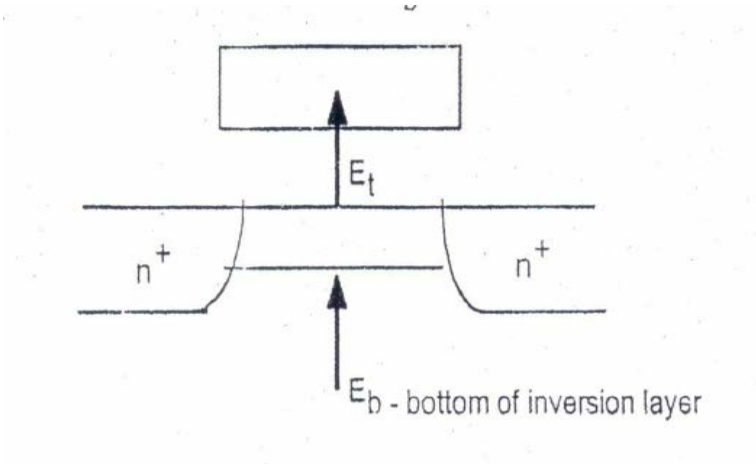
2. (a) (i) What is 'velocity saturation'?

(15 marks)

(ii) What is the relationship of mobility vs vertical field? Draw a figure to describe it.

(15 marks)

(b) Figure below show the Electric field which can affect the mobility of electron.



(i) Derive the effective vertical field as below

$$E_{eff} = \frac{V_g + Vt}{6T_{ox}}$$

(50 marks)

(ii) Given Vg= 0.7 V, V_t =0.5V and T_{ox}= 10 A°

Calculate the effective field. What will be the 'mobility' if the gate of pmos is n-type polysilicon?

(20 marks)

3. (a) Equation A shows the velocity saturation is factored into the basic drain current equation. Equation B includes the velocity saturation.

$$I_d = \frac{1}{1+\frac{V_{ds}}{E_{sat}L}} \frac{WC_{oxe}\mu_{eff}}{L}\left(V_g - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$ ……equation A.

$$I_d \le WQ_{inv}v_{sat}$$ …….. equation B.

If $V_{sat} = \frac{E_{sat}\mu_{eff}}{2}$, derive completely the $I_{dsat} = \frac{WC_{oxe}\mu_{eff}}{2L}\frac{(V_g - V_t)^2}{1+\frac{V_g - V_t}{E_{sat}L}}$ based on equation A and equation B.

(75 marks)

(b) Explain the condition when $E_{sat}L >> V_g - V_t$.

(25 marks)

4. (a) Refer to Figure 4(a),

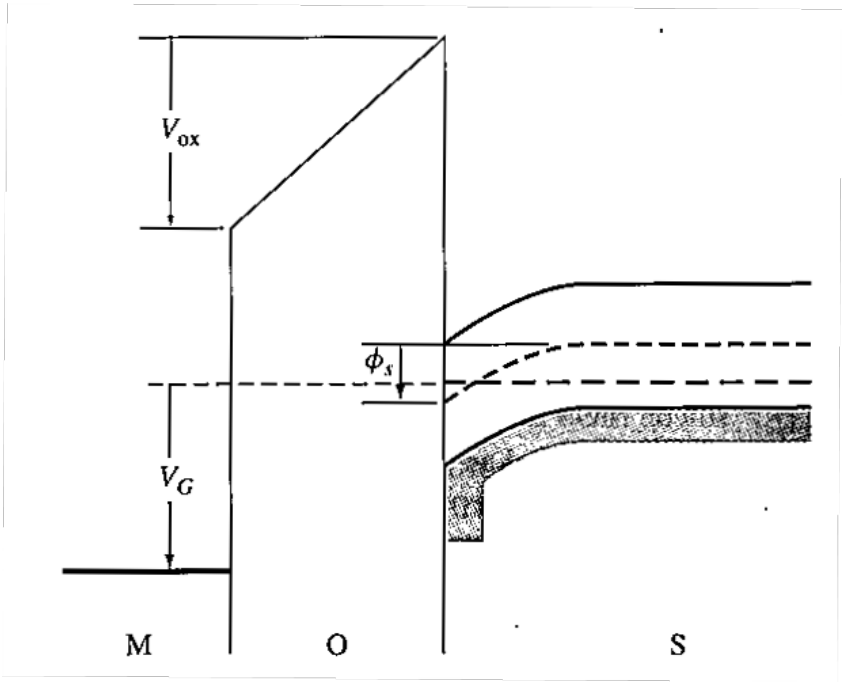


Figure 4(a)

(i) Sketch the charge distribution diagram with an appropriate label.

(ii) Derive the Thereshold voltage for this MOS device.

(30 marks)

(b) Design the oxide thickness of an MOS system to yield specified threshold voltage. Consider an n+ polysilicon gate and p-type silicon substrate doped to $N_a = 5 \times 10^{16} cm^{-3}$. Assume $Q'_{ss} = 10^{11} cm^{-2}$. Determine the oxide thickness such that $V_{TN} = +0.40$ V. (Refer to Appendix 1 and Appendix 2).

(40 marks)

(c) Calculate the semiconductor doping concentration to yield a specified threshold voltage. Consider an aluminium-silicon dioxide-silicon MOS structure. The silicon is n-type, the oxide thickness is $t_{ox} = 650$ Å, and the trapped charge density is $Q'_{ss} = 10^{10}\ cm^{-2}$. Determine the doping concentration such that $V_{TP} = -1.0$ V. Assume $N_d = 2.5 \times 10^{14}\ cm^{-3}$. (Refer to Appendix 1 and Appendix 2).

(30 marks)

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5. (a) Refer to Figure 5(a)

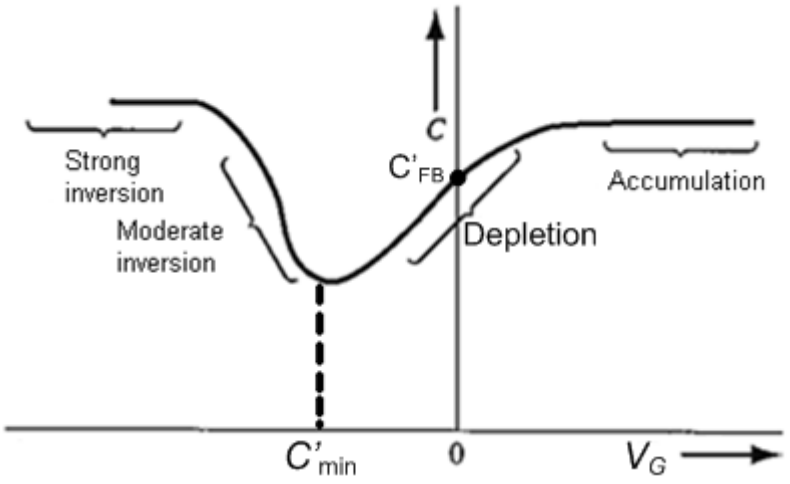

Figure 5(a)

(i) Explain the Figure above based energy diagram and form equation why the capacitance decreases when V_G less than 0.

(ii) Derive the capacitance flat band C'_{FB} and C_{min}

(30 marks)

(b) Define the fixed oxide and interface charge effects

(10 marks)

(c) Refer to Figure 5(b), interprets this measured V_{fb} dependence on oxide thickness. In your answer must have energy band diagram, Q_{ox} and N_d. The gate electrode is N^+ poly-silicon.

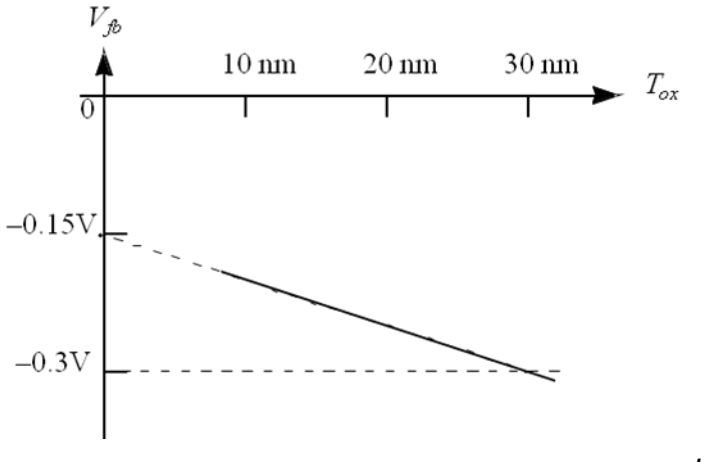

Figure 5(b)

(30 marks)

(d) Calculate C'_{min} and C'_{FB} for MOS capacitor. Consider a p-type silicon substrate at T = 300 K and doped to $N_a = 10^{16}$ cm^{-3}. The oxide is silicon dioxide with thickness of 550 Å and the gate is Aluminium. (Refer to Appendix 2).

(30 marks)

6. (a) Refer to Figure 6(b), explain what do you understand about this modeling image in CMOS fabrication technique. In your explanation, you need to relate with LOCOS process (Local Oxidation of Silicon)

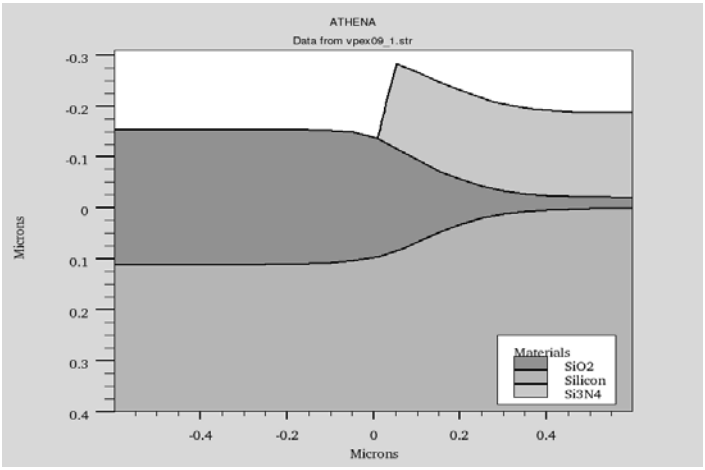

Figure 6(a)

(30 marks)

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(b) Refer to Figure 6(b), explain the function of Ar gas for sputtering process and how this gas affect the deposition of target material on the silicon wafer.

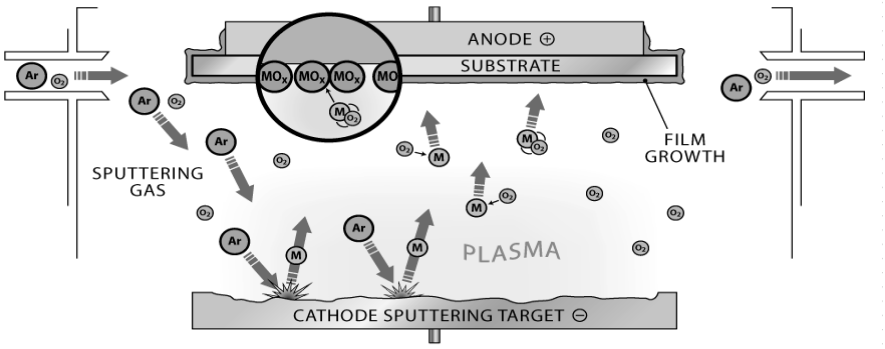

Figure 6(b)

(30 marks)

(c) Define the flip chip packaging technology and 2 advantages compared to wire bonding method.

(20 marks)

(d) Give and explain two failures mode in flip chip packaging technology

(20 marks)

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